AMENDMENTS TO THE CLAIMS:

Please amend claims 2, 10-19 and 22-41 and add newly written claims 42-56 as follows.

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. *(cancelled)*

2. *(currently amended)* An integrated circuit for use as a scheduler of activities to be run on an associated processor, said circuit comprised of: a modular design comprised of an assembly of design tiles, wherein each tile defines a building block having logic and connections, said tiles interconnected to form a two-dimensional array of n rows and m columns which realizes an overall functionality for the integrated circuit, wherein each of the ~~'n'~~n rows of tiles includes a series of stim-wait circuits and provides the control logic for one of ~~'n'~~n schedulable activities and each of the m columns of tiles is arranged to operate one of said stim-wait circuits to a stim condition.

3. *(previously presented)* An integrated circuit as claimed in claim 2 comprising a further row of tiles for interfacing with said associated processor and for generating control signals for said two-dimensional array.

4. *(previously presented)* An integrated circuit as claimed in claim 2 in which the control logic includes means for holding control variables corresponding to each of said activities and

next-activity selection logic for identifying those activities which are ready for running on the processor, depending on the status of said control variables.

5. *(original)* An integrated circuit as claimed in claim 4 in which the control variables include at least one "stim-wait" channel.

6. *(previously presented)* An integrated circuit as claimed in claim 4 including means for setting the control variables comprising a "stim-wait" channel in response to a signal received from an associated processor.

7. *(previously presented)* An integrated circuit as claimed in claim 4 including means for setting the control variables comprising a "stim-wait" channel in response to a signal received from an associated peripheral device.

8. *(previously presented)* An integrated circuit as claimed in claim 4 including means for setting the control variables comprising a stim-wait channel in response to a signal received from a second integrated circuit.

9. *(previously presented)* An integrated circuit as claimed in claim 4 including means for temporarily inhibiting any changes to the control variables from entering the next- activity-selection logic.

10. *(currently amended)* An integrated circuit as claimed in claim 2 and incorporating decoding and encoding logic for routing signals, identifying one or more of said ~~'n'~~n activities, between the associated ~~central~~ processor and the appropriate row of tiles.

11. *(currently amended)* An integrated circuit as claimed in claim ~~2~~4 in which the next-activity[[-]] selection logic includes means for selecting, from said activities which are ready for running, ~~the~~said next activity to be run on a round robin basis.

12. *(currently amended)* An integrated circuit as claimed in claim ~~2~~4 in which ~~the~~said next activity selection logic includes means for allocating differing priority levels to groups of activities, and for selecting from said activities which are ready for running the next activity to run within a group on a round robin basis within that group.

13. *(currently amended)* An integrated circuit as claimed in claim 2 ~~and~~ including means for detecting when a schedulable activity has a higher priority than that activity currently running on an associated ~~central~~ processor and thereby generating an interrupt signal.

14. *(currently amended)* An integrated circuit as claimed in claim 2 ~~and~~ incorporating a counter circuit.

15. *(currently amended)* An integrated circuit as claimed in claim 2 configured for asynchronous operation[[,]] by incorporating ~~level-driven~~level driven, clock-free ripple logic.

16. *(currently amended)* An integrated circuit as claimed in claim 2 ~~and being~~ fabricated using CMOS techniques.

17. *(currently amended)* A processing network comprising at least one processor for controlling~~responsive to~~ an activity scheduler as in claim 22.

18. *(currently amended)* A processing network, as claimed in claim 17, further comprising at least one peripheral device for setting at least one ~~control variable~~control variable in said integrated circuit.

19. *(currently amended)* A multiprocessor network comprising a plurality of processors, each responsive to an activity scheduler as claimed in claim 22, wherein the activity schedulers are operatively linked together.

20. *(Cancelled)*

21. *(Cancelled)*

22. *(currently amended)* An activity scheduler arranged to control activities in a processor, comprising:

an integrated circuit to support shared data and multi-tasking for the processor,

the integrated circuit comprising a set of stim-wait ~~channels~~circuits for each activity ~~and arranged to support a control node mechanism~~,

each stim-wait ~~channel~~circuit responsive to a wait signal and a stim signal to identify when its associated activity is ready to run~~control one of said activities~~, and

the integrated circuit further incorporating next activity logic to select, from the activities ~~identify each activity~~ that ~~is~~are ready to run, the next activity to be run on the processor.

23. *(currently amended)* An activity scheduler arranged to control activities in a plurality of processors, comprising:

a separate integrated circuit to support shared data and multi-tasking for each of said processors,

each integrated circuit comprising a set of stim-wait ~~channels~~circuits for each activity ~~and arranged to support a control node mechanism~~,

each stim-wait ~~channel~~circuit responsive to a wait signal and a stim signal to identify when its associated activity is ready to run ~~control one of said activities~~, and

each of said separate integrated circuits further incorporating next activity logic to ~~identify each~~select the activity that should execute next, from the set of activities ~~activity~~ that ~~is~~are ready to run on the associated processor.

24. *(currently amended)* An activity scheduler, arranged ~~directly~~ to support shared data and multi-tasking in a network of processors, comprising:

a separate ~~integrated~~ circuit to support shared data and multi-tasking in each of said processors,

each ~~integrated~~ circuit being configured to provide~~control~~ a control node mechanism comprising ~~a set of~~ stim-wait ~~channels~~circuits for each activity on an associated processor,

each stim-wait ~~channel~~circuit incorporating holding means to hold a pair of control variables for one of said activities, and

each of said separate ~~integrated~~ circuits further incorporating next activity logic to ~~identify~~ select the activity that should execute next, from the set of activities that are~~each activity that is~~ ready to run on the associated processor.

25. *(currently amended)* An activity scheduler, as claimed in claim 24, in which at least one of said processors is arranged to set at least one control variable in one of said separate ~~integrated~~ circuits.

26. *(currently amended)* An activity scheduler, as claimed in claim 24, including a peripheral device arranged to set at least one control variable in one of said separate ~~integrated~~ circuits.

27. *(currently amended)* An activity scheduler, as claimed in claim 24, in which at least one of said separate ~~integrated~~ circuits is arranged to set at least one control variable in another of said separate ~~integrated~~ circuits.

28. *(currently amended)* An activity scheduler, as claimed in claim 24, in which at least one control node mechanism has its set of stim-wait ~~channels~~circuits arranged as an array comprising n rows and m columns, and at least one of said separate ~~integrated~~ circuits is configured to support said array of control node mechanisms.

29. *(currently amended)* An activity scheduler, as claimed in claim 24, in which the control variables are Boolean.

30. *(currently amended)* An activity scheduler, as claimed in claim 24, including inhibitor means operable to inhibit any changes to control variables from entering the next activity ~~selection~~ logic.

31. *(currently amended)* An activity scheduler, as claimed in claim ~~24~~22, incorporating decoding and encoding logic to identify one or more of said activities and to route signals from said activity scheduler to the appropriate stim-wait circuit~~channel~~.

32. *(currently amended)* An activity scheduler, as claimed in claim ~~24~~22, including activity selection means operable to select the next activity on a round robin basis.

33. *(currently amended)* An activity scheduler, as claimed in claim ~~24~~22, including priority selection means to allocate different priorities to groups of activities and to select the next of said activities within a group on a round robin basis within that group.

34. *(currently amended)* An activity scheduler, as claimed in claim ~~24~~22, including a priority detector to detect an activity having a priority higher that the priority of ~~an~~the activity currently executing ~~being processed~~ on one of said processors, the priority detector being arranged to generate an interrupt signal to interrupt processing of the lower priority activity in favour of the higher priority activity.

35. *(currently amended)* An activity scheduler, as claimed in ~~C~~claim 22, in which the control variables are Boolean.

36. *(currently amended)* A method of controlling activities in a processor comprising holding ~~a plurality of~~ pairs of control variables as stim-wait channels corresponding to such activities, updating said control variables dynamically as said activities execute and interact, and selecting ~~in respect of each activity, identifying~~ the next activity to be run on the processor~~, and selecting the pair of control variables associated with the said next activity~~ dependant on the states of said stim-wait channels as activities execute and interact.

37. *(currently amended)* A method of controlling activities in a plurality of processors comprising holding ~~a plurality of~~ pairs of control variables as stim-wait channels corresponding to such activities, updating said control variables dynamically as said activities execute and interact in each processor, ~~in respect of each activity in each processor, identifying~~ and selecting the next activity to ~~be~~ run on each processor~~, and selecting the pairs of control variables associated with the next activity of each processor~~ dependant on the changing states of said stim-wait channels as activities execute and interact.

38. *(currently amended)* A processing network comprising at least one processor arranged to be controlled by ~~responsive to~~ an activity scheduler as claimed in claim 23.

39. *(currently amended)* A processing network responsive to an ~~activity scheduler~~integrated circuit as claimed in claim 2.

40. *(currently amended)* A processing network, as claimed in claim 38, further comprising at least one peripheral device for setting at least one ~~control variable~~control variable in said integrated circuit.

41. *(currently amended)* A processing network, as claimed in claim 39, further comprising at least one peripheral device for setting at least one ~~control variable~~control variable in said integrated circuit.

42. *(new)* An integrated circuit , for use as a scheduler of activities to be run on an associated processor, said circuit comprising a modular design comprised of an assembly of design tiles, wherein each tile defines a building block having logic and connections, said tiles interconnected to form a two-dimensional array which realizes an overall functionality for the integrated circuit, said array including n rows and m columns wherein each of the n rows of tiles includes a series of stim-wait circuits and provides control logic for one of n schedulable activities, and each of the m columns of tiles is arranged to operate any of the stim-wait circuits in that column to a stimmed condition.

43. *(new*)An integrated circuit, as claimed in claim 42, comprising a further row of tiles for interfacing between said two-dimensional array and said associated processor and for transmitting control signals from said associated processor to said two-dimensional array.

44. *(new)* An integrated circuit, as claimed in claim 42, in which the control logic additionally includes means for holding a set of control variables corresponding to each of said activities, and next-activity selection logic for identifying those activities which are ready for running on said associated processor, depending on the status of said control variables.

45. *(new)* An integrated circuit, as claimed in claim 42, in which each stim-wait circuit is arranged to hold two single-bit control variables 'stim' and 'wait' whose output 'ready' is true when both of said held control variables are true.

46. *(new)* An integrated circuit, as claimed in claim 44, in which said means for holding the set of control variables comprises a stim-wait circuit operable into said stimmed condition or into a waiting condition in response to a signal initiated by an activity running on said associated processor.

47. *(new)* An integrated circuit, as claimed in claim 44, in which said means for holding the set of control variables comprises a stim-wait circuit operable to its said stimmed condition in response to a signal received from an associated peripheral device.

48. *(new)* An integrated circuit, as claimed in claim 44, in which said means for holding the set of control variables comprises a stim-wait circuit operable to its said stimmed condition in response to a signal received from a second integrated circuit.

49. *(new)* An integrated circuit, as claimed in claim 44, including means for temporarily inhibiting any asynchronous changes to said control variables from entering the next-activity selection logic.

50. *(new)* An integrated circuit, as claimed in claim 42 incorporating decoding and encoding logic for routing signals, identifying one or more of said n activities, between said associated processor and the appropriate row of tiles.

51. *(new)* An integrated circuit as claimed in claim 44 in which the next-activity selection logic includes means for selecting, from said activities which are ready for running, said next activity to be run on a round robin basis.

52. *(new)* An integrated circuit as claimed in claim 44 in which said next activity selection logic includes means for allocating differing priority levels to groups of activities, and for selecting from said activities which are ready for running said next activity to run within a group on a round robin basis within that group.

53. *(new)* An integrated circuit as claimed in claim 42 including means for detecting when a schedulable activity has a higher priority than that activity currently running on an associated processor and thereby generating an interrupt signal.

54. *(new)* An integrated circuit as claimed in claim 42 incorporating a counter circuit.

55. *(new)* An integrated circuit as claimed in claim 42 configured for asynchronous operation by incorporating level driven, clock-free ripple logic.

56. *(new)* An integrated circuit as claimed in claim 42 fabricated using CMOS techniques.